REMARKS

Claims 1-29 and 33-37 are pending in the application. No claims have been amended.

Claim Discussion – 35 U.S.C. §102

The Examiner rejected claims 1-27, 29 and 33-37 as being anticipated by Rogers (6,064,407). Applicant respectfully disagrees with the Examiner's rejection. In particular, Rogers fails to teach or suggest "storing portions of the block of data in accordance with the first and second tiled addresses such that selected portions of the block of data are *accessible at the same time* via first and second memory channels" as claimed.

In particular, as noted in the specification on page 5, lines 17-28:

> Embodiments of the present invention provide a method and apparatus for optimally mapping a tiled memory surface to two memory channels, operating in an interleaved fashion, maximizing the memory efficiency of the two channels, while maintaining the desired access granularity. In particular, an incoming request address is used to generate memory addresses for memory channels based on tile and request parameters. The memory controller stores the set of tiled data in the memory in a format such that selected set of tiled data are stored in alternating channels of memory, *such that data blocks are accessible at the same time, as opposed to sequentially*. Thus if the memory controller received a block of data from a source, such as a graphics engine, the memory controller would store portions of the block of data within a single tile in the memory, partitioned such that portions are retrievable via alternate channels of memory at the same time. (Emphasis added.)

Embodiments of the invention allow the memory bandwidth that can be obtained from dual channel memory to be maximized. In contrast, Rogers fails to teach or suggest "storing portions of the block of data in accordance with the first and second tiled addresses such that selected portions of the block of data are *accessible at the same time* via first and second memory channels" as claimed. Rather, Rogers alternates addresses to two channels. This will result in subsequent addresses going to the same channel for rectangular memory operands on X and Y tiles surfaces. **In contrast, embodiments of the invention will send subsequent addresses to two different channels, thereby maximizing efficiency of both the channels.** Step 44, as referred to by the Examiner, fails to disclose selected portions of the block of data being accessible at the same time via first and second memory channels. Step 44 refers to copying data from a source address previously determined to the corresponding tiled address. It does not provide for sending data to two different channels such that data is accessible at the same time.

Claim Discussion – 35 U.S.C. §103

The Examiner rejected claim 28 under 35 USC 103(a) as being unpatentable over Rogers (6,064,407) in view of Chowdhuri et al (6,674,443). Applicant respectfully disagrees with the Examiner's rejection. In particular, both Rogers and Chowdhuri, alone and in combination, fail to teach or suggest "storing portions of the block of data in accordance with the first and second tiled addresses such that selected portions of the block of data are *accessible at the same time* via first and second memory channels" for the reasons noted above.In view of the above, all of the claims are patentable over the cited references.

CONCLUSION

In view of the foregoing, it is respectfully asserted that all of the claims pending in this patent application are in condition for allowance.

The required fee for a three month extension of time is enclosed. Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666.

If the Examiner has any questions, he is invited to contact the undersigned at (323) 654-8218. Reconsideration of this patent application and early allowance of all the claims is respectfully requested.

Respectfully submitted,

Dated: January 24, 2005

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on January 24, 2005.

Margaux Rodriguez *January 24, 2005*